# M.E. Degree

in

VLSI DESIGN

# CURRICULUM & SYLLABUS (CBCS)

**(Innovation and Product Development for sustainability)**

(For students admitted from the Academic Year 2026-2027)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING

CHUNKANKADAI, NAGERCOIL – 629 003.

KANYAKUMARI DISTRICT, TAMIL NADU, INDIA

**St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING,**
**Chunkankadai, Nagercoil – 629 003**
**AUTONOMOUS COLLEGE AFFILIATED TO ANNA UNIVERSITY**
**ACADEMIC REGULATIONS 2026**
**M.E. VLSI DESIGN CURRICULUM**
**CHOICE BASED CREDIT SYSTEM**

## VISION OF THE INSTITUTION

To be a centre of excellence in engineering education and research for a technically empowered humane society.

## MISSION OF THE INSTITUTION

**M1:** Foster a vibrant academic environment for learning fundamental concepts, emerging technologies, and research-oriented practices.
**M2:** Cultivate personal maturity and professional skills through stimulating coaching and practical training.
**M3:** Provide inspiring high calibre faculty to mentor students from diverse backgrounds, especially the underprivileged.
**M4:** Create ample opportunities to transform rural youth into top class professionals and technocrats, capable of serving at the local and global levels with ethical integrity.

## VISION OF THE PROGRAMME

Developing technically competent Electronics and Communication Engineers with academic excellence, innovative research, ethical standards and international outlook to serve the society

## MISSION OF THE PROGRAMME

**M1.** To provide quality teaching in order to produce graduates with academic excellence, technical competence and ethical values.
**M2.** To develop advanced professionalism and exceptional career growth through inspiring faculty members and excellent infrastructure.
**M3.** To create awareness on state of the art technologies through research and industry-institute collaboration.
**M4.** To inculcate a sense of innovation and commitment among the students to apply knowledge and technologies for the benefit of the society.

## PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

| | |
|---|---|
| **I.** | Apply technical knowledge and skills to have successful career in industry, government and academia as VLSI engineers. |
| **II.** | Pursue multidisciplinary scientific research in VLSI and related areas for the benefits of society. |
| **III.** | Make use of various state-of art systems and cutting-edge technologies to solve various complex engineering problems. |
| **IV.** | Inculcate leadership skills, team work, effective communication and lifelong learning to the success of their organization and nation. |
| **V.** | Practice ethics and exhibit commitment in profession to empower / enable rural communication infrastructure. |

## PROGRAMME OUTCOMES (POs)

| PO | Programme Outcomes |
|---|---|
| 1 | Independently carry out research/investigation and development work to solve practical problems. |
| 2 | Write and present substantial technical report/document. |
| 3 | Demonstrate a degree of mastery over the techniques in the area of analog and digital VLSI system design. |
| 4 | Analyze and design the subsystems in RF, signal processing, modern communication systems and networks. |
| 5 | Solve problems in analog and digital system design using advanced hardware and software tools. |
| 6 | Interact effectively with the technical experts in industry and society. |

## KNOWLEDGE AND ATTITUDE PROFILE (WK)

**WK1:** A systematic, theory-based understanding of the natural sciences applicable to the discipline and awareness of relevant social sciences.
**WK2:** Conceptually-based mathematics, numerical analysis, data analysis, statistics and formal aspects of computer and information science to support detailed analysis and modelling applicable to the discipline.
**WK3:** A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline.
**WK4:** Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline.

**WK5:** Knowledge, including efficient resource use, environmental impacts, whole-life cost, re use of resources, net zero carbon, and similar concepts, that supports engineering design and operations in a practice area.

**WK6:** Knowledge of engineering practice (technology) in the practice areas in the engineering discipline.

**WK7:** Knowledge of the role of engineering in society and identified issues in engineering practice in the discipline, such as the professional responsibility of an engineer to public safety and sustainable development.

**WK8:** Engagement with selected knowledge in the current research literature of the discipline, awareness of the power of critical thinking and creative approaches to evaluate emerging issues.

**WK9:** Ethics, inclusive behavior and conduct. Knowledge of professional ethics, responsibilities, and norms of engineering practice. Awareness of the need for diversity by reason of ethnicity, gender, age, physical ability etc. with mutual understanding and respect, and of inclusive attitudes.

**PEO's – PO's MAPPING**

| PROGRAMME EDUCATIONAL OBJECTIVES | PROGRAMME OUTCOMES | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| I. | 2 | 1 | 2 | 3 | 3 | 2 |
| II. | 2 | 1 | 2 | 3 | 3 | 2 |
| III. | 2 | 1 | 2 | 3 | 3 | 2 |
| IV. | 2 | 1 | 2 | - | - | - |
| V. | 1 | 1 | 2 | - | - | 2 |

**PROGRAMME ARTICULATION MATRIX**

| Year | Semester | Course name | PO | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 |
| I | I | Induction Programme | 2 | 2 | 2 | - | - | - |
| | | Optimization Techniques and Graph Algorithm for VLSI Engineering | 3 | - | 1 | 2 | 2 | - |
| | | ASIC and FPGA Design | 1 | 1 | 2 | 1 | 2 | 2 |
| | | Advanced Digital System Design | 3 | 1 | 3 | 1 | 2 | 1 |
| | | Analog Integrated Circuit Design | 1 | 1 | 2 | 2 | 1 | 1 |
| | | Research Methodology and Intellectual Property Rights | 3 | 3 | 2 | 2 | 2 | 2 |
| | | Research Tool Laboratory | 2 | 2 | 2 | 3 | 3 | 2 |
| | | Analog IC Design Laboratory | 2 | 1 | 2 | 3 | 2 | 1 |
| | | Technical Seminar | 3 | 2 | 3 | 2 | 2 | 3 |
| I | II | Semiconductor Devices and Modeling | 2 | 2 | 1 | 2 | 2 | 2 |
| | | VLSI testing and verification using UVM | 2 | 1 | 3 | 3 | 2 | 1 |
| | | Low Power VLSI Design | 2 | 1 | 2 | 2 | 2 | 1 |
| | | Verification using UVM Laboratory | 2 | 1 | 3 | 2 | 2 | 1 |

**SUSTAINABLE DEVELOPMENT GOALS**

**GOAL 1: No Poverty**
End poverty in all its forms everywhere (eradicate extreme poverty currently measured as people living on less than $1.25 a day.)
**GOAL 2: Zero Hunger**
End hunger, achieve food security and improved nutrition and promote sustainable agriculture
**GOAL 3: Good Health and Well-being**
Ensure healthy lives and promote well-being for all at all ages
**GOAL 4: Quality Education**
Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all
**GOAL 5: Gender Equality**
Achieve gender equality and empower all women and girls
**GOAL 6: Clean Water and Sanitation**
Ensure availability and sustainable management of water and sanitation for all
**GOAL 7: Affordable and Clean Energy**
Ensure access to affordable, reliable, sustainable and modern energy for all

**GOAL 8: Decent Work and Economic Growth**

Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all

**GOAL 9: Industry, Innovation and Infrastructure**

Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation

**GOAL 10: Reduced Inequality**

Reduce inequality within and among countries

**GOAL 11: Sustainable Cities and Communities**

Make cities and human settlements inclusive, safe, resilient and sustainable

**GOAL 12: Responsible Consumption and Production**

Ensure sustainable consumption and production patterns

**GOAL 13: Climate Action**

Take urgent action to combat climate change and its impacts

**GOAL 14: Life Below Water**

Conserve and sustainably use the oceans, seas and marine resources for sustainable development

**GOAL 15: Life on Land**

Protect, restore and promote sustainable use of terrestrial ecosystems, sustainably manage forests, combat desertification, and halt and reverse land degradation and halt biodiversity loss

**GOAL 16: Peace and Justice Strong Institutions**

Promote peaceful and inclusive societies for sustainable development, provide access to justice for all and build effective, accountable and inclusive institutions at all levels

**GOAL: 17: Partnership to achieve the goal**

Strengthen the means of implementation and revitalize the global partnership for sustainable development

## SEMESTER: I

Number of Courses: **08**
Total Credits: **24**

| Course Code | Course Title | Course Type | Classroom Instruction(CI) (in Hours per Semesters) | | Lab Instruction(LI) (in Hours per Semesters) | Team Work(TW) and Self Learning(SL) (in Hours per Semesters) | Total Number of Hours (in Hours per Semesters) | Total Credits (C)=(Total Hours/30) | SDG Goal Mapped | Category |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | | | | | |
| IP26C07 | Induction Programme* | IP | 24 | 0 | 0 | 6 | 30 | 0 | 4,8,9, 16, 17 | IP |
| MA26105 | Optimization Techniques and Graph Algorithm for VLSI Engineering | TC | 45 | 15 | 0 | 60 | 120 | 4 | 4,8,9,11 | BSC |
| VL26101 | ASIC and FPGA Design | TCP | 45 | 0 | 30 | 45 | 120 | 4 | 3,4,9,11 ,12 | PCC |
| VL26102 | Advanced Digital System Design | TC | 45 | 15 | 0 | 60 | 120 | 4 | 1,2,3,7 | PCC |
| VL26103 | Analog Integrated Circuit Design | TC | 45 | 0 | 0 | 45 | 90 | 3 | 4,7,9,12,13 | PCC |
| RM26C01 | Research Methodology and Intellectual Property Rights | TC | 45 | 15 | 0 | 60 | 120 | 4 | 1,2,3,7 | FC |
| RM26C02 | Research Tool Laboratory | PC | 0 | 0 | 60 | 0 | 60 | 2 | 4,9,16, 17 | FC |
| VL26104 | Analog IC Design Laboratory | PC | 0 | 0 | 60 | 0 | 60 | 2 | 4,7,9,12,13 | PCC |
| VL26105 | Technical Seminar** | - | 0 | 0 | 30 | 0 | 30 | 1 | 4,8,9,16,17 | EEC |
| **Total** | | | **225** | **45** | **180** | | | **24** | | |

* - Refer clause 21 in regulation 2026. The evaluation procedure is detailed in the syllabus.
** - Internally Evaluated Course. The evaluation procedure is detailed in the syllabus.

## SEMESTER: II

Number of Courses: **8**
Total Credits: **20**

| Course Code | Course Title | Course Type | Classroom Instruction(CI) (in Hours per Semesters) | | Lab Instruction(LI) (in Hours per Semesters) | Team Work(TW) and Self Learning(SL) (in Hours per Semesters) | Total Number of Hours (in Hours per Semesters) | Total Credits (C)=(Total Hours/30) | SDG Goal Mapped | Category |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | | | | | |
| VL26201 | Semiconductor Devices and Modeling | TC | 45 | 0 | 0 | 45 | 90 | 3 | 7,9,12, 13 | PCC |
| VL26202 | VLSI Testing and Verification using UVM | TC | 45 | 0 | 0 | 45 | 90 | 3 | 4,8,9 | PCC |
| VL26203 | Low Power VLSI Design | TCP | 45 | 0 | 30 | 45 | 120 | 4 | 4,7,9,12 | PCC |
| VL26204 | Verification using UVM Laboratory | PC | 0 | 0 | 60 | 0 | 60 | 2 | 4,9,12 | PCC |
| | Open Elective I | TC | 45 | 0 | 0 | 45 | 90 | 3 | | OEC |
| | Professional Elective I | TC | 45 | 0 | 0 | 45 | 90 | 3 | | PEC |
| VL26S01 | Industry Collaborated Course I* | - | 15 | 0 | 15 | 0 | 30 | 1 | | ICC |
| VL26S02 | Self Learning Course * | - | 0 | 0 | 0 | 30 | 30 | 1 | | SLC |
| **Total** | | | **240** | **0** | **105** | | | **20** | | |

* - Evaluation and certification by course offering body.

## SEMESTER II, OPEN ELECTIVE I

| Course Code | Course Title | Course Type | Classroom Instruction (CI) (in Hours per Semesters) | | Lab Instruction(LI) (in Hours per Semesters) | Term Work(TW) and Self Learning(SL) (in Hours per Semesters) | Total Number of Hours (in Hours per Semesters) | Total Credits (C)=(Total Hours/30) | SDG Goal Mapped | Category |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | | | | | |
| VL26901 | VLSI Technology | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3, 4, 8, 9 | OEC |
| VL26902 | Embedded Sysem Design | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3, 4, 8, 9 | OEC |

## SEMESTER II, PROFESSIONAL ELECTIVES – I

| Course Code | Course Title | Course Type | Classroom Instruction(CI) (in Hours per Semesters) | | Lab Instruction(LI) (in Hours per Semesters) | Team Work(TW) and Self Learning(SL) (in Hours per Semesters) | Total Number of Hours (in Hours per Semesters) | Total Credits (C)=(Total Hours/30) | SDG Goal Mapped | Category |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | | | | | |
| VL26001 | Digital CMOS VLSI Design | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3,4,8, 9 | PEC |
| VL26002 | RF IC Design | TC | 45 | 0 | 0 | 45 | 90 | 3 | 4,7,9,11,12 | PEC |
| VL26003 | Electromagnetic Interference and Compatibility | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3,7,9,11, 12 | PEC |
| VL26004 | Physical Design of VLSI | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3,9,12 | PEC |
| VL26005 | Hardware Software Co Design for FPGA | TC | 45 | 0 | 0 | 45 | 90 | 3 | 7,9,12,13 | PEC |
| VL26006 | CAD for VLSI Design | TC | 45 | 0 | 0 | 45 | 90 | 3 | 3, 4, 8, 9 | PEC |

## SEMESTER I

| IP26C07 | Induction Programme | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 24 | 0 | 0 | 6 | 30 | 0 | 4,8,9, 16,17 |

**COURSE OBJECTIVES:**

- To familiarize students with institutional policies, academic regulations, and programme structure.
- To introduce research methodology, ethical practices, and emerging engineering trends.
- To develop communication, technical writing, and presentation skills.
- To create awareness about career opportunities, higher education, and industry expectations.
- To inculcate professional ethics, teamwork, and leadership qualities.

**COURSE CONTENT:**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 1** | **Institutional Orientation** | **4** | **0** | **0** | **1** | **5** | | **4** |

Vision, Mission, and Quality Policy – Organizational structure – Campus facilities – Library, laboratory, and IT infrastructure – Student support systems – Interaction with faculty and peers.
**Activities:** Campus Resource Mapping and Group Presentation.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 2** | **Academic Regulations & Programme Structure** | **4** | **0** | **0** | **1** | **5** | | **4,9** |

Choice Based Credit System (CBCS) – Curriculum framework – Credit requirements – Evaluation and assessment procedures – Attendance norms – Examination system – Academic integrity guidelines.
**Activities:** Preparation of Individual Academic Plan.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Research Methodology & Emerging Technologies** | **8** | **0** | **0** | **2** | **10** | | **4** |

Research process – Problem identification – Literature review – Research ethics and plagiarism – Overview of emerging technologies (AI, Data Science, IoT, etc.) – Interdisciplinary research opportunities.
**Activities:** Mini Research Problem Identification and Presentation.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Skill Development & Career Planning** | **4** | **0** | **0** | **1** | **5** | | **8** |

Communication skills – Technical writing – Presentation skills – Resume preparation – Career opportunities – Higher studies – Competitive exams – Internship and placement readiness.
**Activities:** Resume Preparation and Elevator Pitch Presentation.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **Professional Development & Well-Being** | **4** | **0** | **0** | **1** | **5** | | **16,17** |

Engineering ethics – Professional values – Teamwork and leadership – Innovation and entrepreneurship – Startup ecosystem – Time management – Stress management – Counseling and mentoring support.
**Activities:** Case Study Analysis on Ethics and Teamwork.

| COURSE OUTCOMES: | |
|---|---|
| **At the end of the course, the students will be able to:**<br>CO1: Apply institutional policies and academic regulations to manage postgraduate studies effectively.<br>CO2: Apply research methodologies and ethical principles to identify research problems.<br>CO3: Demonstrate communication, technical writing, and presentation skills.<br>CO4: Analyze career opportunities and industry expectations for informed decision-making.<br>CO5: Apply professional ethics and teamwork skills in academic and organizational environments. | |
| **Weightage:** Continuous Assessment: 100% | |
| **Assessment Methodology:** Active Participation (40%), Assignments (30%), Quiz (30%) | |
| **REFERENCES:** | |
| 1. | Johri, A., "International Handbook of Engineering Education Research", Taylor & Francis, 2023. |
| 2. | Murthy, D. N. P., & Page, N. W., "Education and Research for the Future", Springer, 2023. |
| 3. | Oliveira, T. A., & Hebebci, M. T. (Eds.), "Current Academic Studies in Technology and Education 2024", ISRES Publishing, 2024. |
| 4. | Kannan, R., Thirumalai, P., & Geetha, T. V. (Eds.), Proceedings of the International Conference on Technology for Education (T4E 2024), Springer, 2024. |
| 5. | Rajesh, S., Raghu Prasad, B. K., & Praveen, K. V. (Eds.), Recent Advances in Sustainable Construction Technology, Geotechnics and Structural Engineering", Springer, 2026. |
| **E resources/E materials:** | |
| 1. | https://alison.com/course/essentials-of-research-methodology |
| 2. | https://www.coursera.org/learn/research-methodologies |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | **PO1 (Research Capability)** | **PO2 (Technical Communication)** | **PO3 (Domain Mastery)** |
|---|---|---|---|
| **CO1** | 2 | 1 | 2 |
| **CO2** | 3 | 2 | 2 |
| **CO3** | 1 | 3 | 1 |
| **CO4** | 2 | 2 | 2 |
| **CO5** | 1 | 2 | 1 |
| **CO** | 2 | 2 | 2 |

| MA26105 | Optimization Techniques and Graph Algorithm for VLSI Engineering | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 15 | 0 | 60 | 120 | 4 | 4,9,11,13 |

**COURSE OBJECTIVES:**

- To familiarize the students with the formulation and construction of a mathematical Model for a linear programming problem in a real-life situations.
- To develop student's ability to formulate and solve real-world optimization problems using transportation and assignment models
- To understand the applications of Simulation modeling techniques to solve real-life problems.
- To introduce graph as mathematical model to solve connectivity problems.
- To introduce fundamental graph algorithms

**COURSE CONTENT:**

| Unit 1 | Linear Programming | 9 | 3 | 0 | 12 | 24 | | 4,7,9 |
|---|---|---|---|---|---|---|---|---|

Formulation of liner programming problem – Graphical method of solution – Canonical and standard form of liner programming problem – Simplex method – Artificial variables: Big-M method.

**Activity:** Formulate and solve VLSI resource optimization using linear programming.

| Unit 2 | Transportation and Assignment Models | 9 | 3 | 0 | 12 | 24 | | 4,9,13 |
|---|---|---|---|---|---|---|---|---|

Definition of the transportation model – Mathematical formulation of transportation models – Basic feasible solution: Vogel's approximation method – Optimal solution by modified distribution (MODI) method – Definition of the assignment model – Mathematical formulation of assignment models – Hungarian method for solution of the assignment problem.

**Activity:** Create a transportation model by cost/time to optimize in VLSI industry and create an assignment model by assigning optimal allocation of VLSI resources

| Unit 3 | Simulation | 9 | 3 | 0 | 12 | 24 | | 4,9 |
|---|---|---|---|---|---|---|---|---|

Discrete event simulation – Monte Carlo simulation – Use of random numbers – Generation of random numbers.

**Activity:** Evaluate circuit reliability uses Monte Carlo simulation and random number generation to model uncertainties.

| Unit 4 | Graphs | 9 | 3 | 0 | 12 | 24 | | 4,9 |
|---|---|---|---|---|---|---|---|---|

Graphs and graph models - Graph terminology and special types of graphs -Matrix representation of graphs and graph isomorphism - Introduction to Trees - Spanning trees - Connectivity- Euler and Hamilton paths (Definition and Problems)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Activity:** Routing VLSI problems using spanning trees, Euler and Hamilton paths. | | | | | | | | |
| **Unit 5** | **Graph Algorithm** | **9** | **3** | **0** | **12** | **24** | | **4,9,11** |
| Traversal - Depth-First search -Breadth-First search on a graph, -Shortest path algorithms: Dijkstra's Algorithm- Minimum cost Spanning tree - Prims Algorithm, Kruskal Algorithm.<br>**Activity:** Graph Traversal using DFS and BFS (VLSI Interconnect Analysis). | | | | | | | | |
| **COURSE OUTCOMES:** | | | | | | | | |
| **At the end of the course, the students will be able to:**<br>CO1: Apply the graphical method, simplex method and artificial variables to solve linear programming problems and optimal solutions.<br>CO2: Solve transportation problems using Modified Distribution method, and assignment problems using the Hungarian Method to obtain optimal allocation results.<br>CO3: Apply simulation methods to real-world problems.<br>CO4: Apply graph as mathematical model to solve connectivity problems.<br>CO5: Apply fundamental graph algorithms including shortest path and traversal techniques. | | | | | | | | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | | | | | | | | |
| **Assessment Methodology:** Internal Examinations (70%) and Activity (30%) | | | | | | | | |
| **REFERENCES:** | | | | | | | | |
| 1. | Taha H.A., "Operations Research: An Introduction", Pearson Education, New Delhi, Eleventh edition, 2022. | | | | | | | |
| 2. | Kanti Swarup, P. K. Gupta and Man Mohan., "Operation Research", Sultan Chand & Sons, Twentieth Revised Edition, 2022. | | | | | | | |
| 3. | Balakrishna, R and Ranganathan. K., "A textbook of graph theory", Springer Science and Business Media", 2021. | | | | | | | |
| 4. | Deo, N., "Graph theory with applications to engineering and computer science" Dover Publications, Inc.2021. | | | | | | | |
| 5. | West., D. B., "Introduction to graph theory", Pearson Education, 2020. | | | | | | | |
| **E resources/E materials:** | | | | | | | | |
| 1. | https://allen.in/jee/maths/graphical-method-linear-programming | | | | | | | |
| 2. | https://nptel.ac.in/courses/110106062 | | | | | | | |
| 3. | https://github.com/afrid18/Data_structures_and_algorithms_in_cpp | | | | | | | |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| CO1 | 3 | - | 1 | 2 | 2 | - |
| CO2 | 3 | - | 1 | 2 | 2 | - |
| CO3 | 3 | - | 1 | 2 | 2 | - |
| CO4 | 3 | - | 1 | 2 | 2 | - |
| CO5 | 3 | - | 1 | 2 | 2 | - |
| CO | 3 | - | 1 | 2 | 2 | - |

| VL26101 | ASIC and FPGA Design | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 0 | 30 | 45 | 120 | 4 | 3,4,9,11,12 |

**COURSE OBJECTIVES:**

- To learn the architecture of FPGA and perform its implementation
- To study the design flow and of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To design and test digital circuits using programming tools for front end chip design.
- To gain knowledge about ASIC physical design using CAD tools for back-end

**COURSE CONTENT:**

| Unit 1 | FPGA and Implementation Techniques | 9 | 0 | 6 | 9 | 24 | | 9,12 |
|---|---|---|---|---|---|---|---|---|

FPGA, types and Architecture, RTL Coding, Timing Closure & Constraints, High-Level Synthesis, System Integration & High-Speed Interfaces, AI in FPGA Design.

**Activities:** 1. Design and implement a simple combinational circuit on an FPGA development board and analyze routing

**Practical Experiments:**

1. Build a 32-bit ALU using a Finite State Machine (FSM) controller to schedule data access to the shared resources.

| Unit 2 | ASIC Design Fundamentals | 9 | 0 | 6 | 9 | 24 | | 3,9,12 |
|---|---|---|---|---|---|---|---|---|

Types of ASICs: Full custom, Semicustom and Programmable ASICs, ASIC design flow, Sequential and combinational design elements: Blocking vs. non-blocking assignments, Timing constraints.

**Activities:** 1. Analyze and classify different types of ASICs based on their applications and design complexity.

**Practical Experiments:**

1. Simulate CMOS inverter circuits and study transistor parasitic effects using a circuit simulator tool.

2. Experiment with 2 state and 4 state data types.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Programmable ASIC, Logic Cells and Architectures** | **9** | **0** | **6** | **9** | **24** | | **9,11,12** |

Programming technolgies: Antifuse, SRAM, EPROM, EEPROM, Datapath elements, Combinational and sequential logic cells, Micro-architecture design strategies, Multiple clock domains, low-power techniques.

**Activities:**1. Compare different programmable ASIC technologies (Antifuse Vs SRAM Vs EPROM) in terms of speed, power and programmability.

**Practical Experiments:**

1. Model and verify simple ALU
2. Model and verify an instruction stack

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Synthesis and Optimization** | **9** | **0** | **6** | **9** | **24** | | **4,9,12** |

Optimization techniques using RTL tweaks, common synthesis compilation strategies, constraint definition, practical synthesis workflows using standard EDA tools.

**Activities:** 1. Write simple Verilog/VHDL modules and synthesize them using logic synthesis tools.

**Practical Experiments:**

1. Use an interface between testbench and DUT
2. Develop a test program
3. Create a simple and advanced testbench.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **ASIC Physical Design and Signoff** | **9** | **0** | **6** | **9** | **24** | | **4,9,12** |

Physical Design & Signoff: Design for Testability (DFT), static timing analysis (STA), Placement and Routing, Physical Verification and signoff.

**Activities**: 1. Case study: ASIC Implementation of sequential circuits and verify design rule compliances.

**Practical Experiments:**

1.Create a scoreboard using dynamic array
2.Use mailboxes for verification

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Develop combinational circuits using FPGA and analyze the area, power and speed.
CO2: Articulate ASIC types, design flow, and timing analysis.
CO3: Apply data path elements to design and analyze combinational and sequential logic cells.
CO4: Utilize EDA tool for logic synthesis in front end chip design.
CO5: Analyze ASIC physical design using EDA tool for back-end chip design.

**Weightage:** Continuous Assessment: 50%, End Semester Examinations: 50%

**Assessment Methodology:** Theory (30%), Practical (10%), Activities (10%), End Semester Theory Examinations: 50%

| REFERENCES: | |
|---|---|
| 1. | Vaibbhav Taraate, “ASIC Design and Synthesis: RTL Design using Verilog”, Springer, 2021. |
| 2. | Kevin Hubbard, “Mastering FPGA Chip Design: For Speed, Area, Power, and Reliability”, Elektor International Media, 2025. |
| 3. | Shirshendu Roy, “Advanced Digital System Design A Practical Guide to Verilog Based FPGA and ASIC Implementation”, Springer, 2024. |
| 4. | Sheetal Umesh Bhandari, Anuradha D. Thakare, “Artificial Intelligence Applications and Reconfigurable Architectures”, Wiley, 2023. |
| **E resources/E materials:** | |
| 1. | https://vlsitalks.com/ |
| 2. | https://www.wevolver.com/article/the-ultimate-guide-to-asic-design-from-concept-to-production |
| 3. | https://anysilicon.com/asic-design-from-spec-to-chips/ |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 1 | 1 | 2 | 1 | 2 | 2 |
| **CO2** | 1 | 1 | 2 | 1 | 2 | 2 |
| **CO3** | 1 | 1 | 2 | 1 | 2 | 2 |
| **CO4** | 1 | 1 | 2 | 1 | 2 | 2 |
| **CO5** | 1 | 1 | 2 | 1 | 2 | 2 |
| **CO** | 1 | 1 | 2 | 1 | 2 | 2 |

| **VL26102** | **Advanced Digital System Design** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **15** | **0** | **60** | **120** | **4** | **1,2,3,7** |

**COURSE OBJECTIVES:**

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

**COURSE CONTENT:**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 1** | **Sequential Circuit Design** | **9** | **0** | **3** | **12** | **24** | | **1,3** |

State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts

**Activities:** 1. Design state diagrams for given problems
2. Implement synchronous circuits using ASM

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 2** | **Asynchronous Sequential Circuit Design** | **9** | **0** | **3** | **12** | **24** | | **3,7** |

Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.

**Activities:** 1. Analyze and minimize flow tables
2. Identify and eliminate hazards

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Fault Diagnosis and Testability Algorithms** | **9** | **0** | **3** | **12** | **24** | | **2,7** |

Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.

**Activities:** 1. Generate fault tables for combinational circuits
2. Simulate fault detection using D-algorithm

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Synchronous Design Using Programmable Devices** | **9** | **0** | **3** | **12** | **24** | | **2,7** |

PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).

**Activities:** 1. Implement FSM using PLA/PAL
2. Program and simulate FSM on FPGA

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **System Design Using Verilog** | **9** | **0** | **3** | **12** | **24** | | **1,2,7** |

Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, testbenches, combinational/sequential circuit realization.

**Activities:** 1. Write and simulate Verilog code for registers, counters, serial adders
2. Design and test a simple microprocessor in Verilog.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Analyze and design sequential circuits using state diagrams and ASM charts.
CO2: Make use of the fundamentals of asynchronous sequential circuits.
CO3: Apply fault diagnosis and testability algorithms to digital circuits
CO4: Design of synchronous circuits using programmable devices.

| | |
|---|---|
| CO5: Develop and simulate digital systems using Verilog HDL and FPGA. | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) | |
| **REFERENCES:** | |
| 1. | Charles H. Roth Jr. and Larry L. Kinney, "Fundamentals of Logic Design", Seventh Edition, Cengage Learning, 2020. |
| 2. | M. Morris Mano and Michael D. Ciletti, "Digital Design with an Introduction to the Verilog HDL, VHDL, and System Verilog", Sixth Edition, Pearson Education, 2022. |
| 3. | Vaibbhav Taraate, "Digital Logic Design Using Verilog: Coding and RTL Synthesis", Second Edition, Springer Singapore, 2022. |
| 4. | Shirshendu Roy, "Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation", Springer Cham, 2024. |
| 5. | Suman Lata Tripathi, Sobhit Saxena, Sanjeet K. Sinha, and Govind S. Patel, "Digital VLSI Design and Simulation with Verilog", Wiley, 2021. |
| **E resources/E materials:** | |
| 1. | https://www.xilinx.com/ |
| 2. | https://www.veripool.org/wiki/verilator |
| 3. | IEEE Transactions on VLSI Systems (TVLSI) |
| 4. | IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) |
| 5. | IEEE Transactions on Digital Circuits and Systems |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | - | 3 | 1 | 2 | 1 |
| **CO2** | 2 | - | 3 | 1 | 2 | 1 |
| **CO3** | 3 | 1 | 3 | 1 | 2 | 1 |
| **CO4** | 3 | 1 | 2 | 1 | 3 | 1 |
| **CO5** | 3 | 2 | 3 | 1 | 3 | 1 |
| **CO** | 3 | 1 | 3 | 1 | 2 | 1 |

| VL26103 | Analog Integrated Circuit Design | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 0 | 0 | 45 | 90 | 3 | 4,7,9,12 ,13 |

**COURSE OBJECTIVES:**

- To learn the basics of single stage analog CMOS amplifiers
- To gain knowledge in noise characteristics of amplifiers
- To study the performance parameters of amplifiers and compensation techniques
- To design an analog amplifier with bandgap reference

**COURSE CONTENT:**

| Unit 1 | Single Stage Amplifiers | 9 | 0 | 0 | 9 | 18 | | 4,7,9,12 |
|---|---|---|---|---|---|---|---|---|

Basic MOS physics and equivalent circuits and models - CS, CG and Source Follower- differential amplifier with active load- Cascode and Folded Cascode configurations with active load- design of Differential and Cascode Amplifiers- to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

**Activities:**1. Case study: Design and implementation of CS, CG amplifiers.

2. Quiz: Fundamentals of single stage amplifiers.

| Unit 2 | High Frequency and Noise Characteristics of Amplifiers | 9 | 0 | 0 | 9 | 18 | | 4,7,9,12 |
|---|---|---|---|---|---|---|---|---|

Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

**Activities:**1. Case study: Analyze frequency response of CS, CG and source follower.

2. Case study: Noise in amplifiers.

| Unit 3 | Feedback and Operational Amplifiers | 9 | 0 | 0 | 9 | 18 | | 4,7,9,12 |
|---|---|---|---|---|---|---|---|---|

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, Single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

**Activities:** 1. Case study: Design and implement negative feedback circuits

2. Concept map activity: Connecting Op-Amp Performance Parameters

| Unit 4 | Stability and Frequency Compensation | 9 | 0 | 0 | 9 | 18 | | 4,7,9,12 |
|---|---|---|---|---|---|---|---|---|

General considerations, Multiple systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

**Activities**:1. Case study: Analyze phase margin and stability in two-stage op-amps

2. Research paper writing: Stability and Frequency Compensation Techniques in Multi-Stage Op-Amps.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **Band Gap Reference** | **9** | **0** | **0** | **9** | **18** | | **4,7,9,12 ,13** |

Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, Constant $G_m$ biasing, BGR under low voltage conditions.

**Activities:** 1. Case study: Design of BGR under low voltage conditions.

2. Research paper writing: Low-Voltage Bandgap and PTAT-Based Biasing Techniques in Analog IC Design.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Design single stage analog CMOS amplifiers.

CO2: Analyze the noise characteristics and frequency response of single stage amplifiers.

CO3: Develop negative feedback circuits.

CO4: Demonstrate the compensation techniques in Op Amps.

CO5: Design bandgap reference circuits.

**Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60%

**Assessment Methodology:** Internal Assessment (70%), Activities (30%)

**REFERENCES:**


| | |
|---|---|
| 1. | Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Second Edition, McGraw Hill Education, 2020. |
| 2. | Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, "Analysis and Design of Analog Integrated Circuits", Sixth Edition, Wiley, 2024. |
| 3. | Paul G. A. Jespers, Boris Murmann, "Systematic Design of Analog CMOS Circuits", Cambridge University press, 2022. |
| 4. | Phillip E, Allen, Douglas R, Holberg, "CMOS Analog Circuit Design", Third Edition, Oxford University Press, 2020. |
| 5. | James M. Fiore, "Operational Amplifiers & Linear Integrated Circuits: Theory and Application", Third Edition, West Publishing, 2021. |


**E resources/E materials:**

| | |
|---|---|
| 1. | NPTEL Analog IC Design Course - video lectures and study material |
| 2. | https://youtu.be/xeEQdo5MOGo?si=dkn2TDkP4lVZfNXN |
| 3. | https://youtu.be/gDmH-Kgrc-E?si=xq_Rb_yl1cz8xWNz |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 1 | 1 | 2 | 2 | 1 | 1 |
| **CO2** | 1 | 1 | 2 | 2 | 1 | 1 |
| **CO3** | 1 | 1 | 2 | 2 | 1 | 1 |
| **CO4** | 1 | 1 | 2 | 2 | 1 | 1 |
| **CO5** | 1 | 1 | 2 | 2 | 1 | 1 |
| **CO** | 1 | 1 | 2 | 2 | 1 | 1 |

| **RM26C01** | **Research Methodology and Intellectual Property Rights** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **15** | **0** | **60** | **120** | **4** | **1,2,3,7** |

**COURSE OBJECTIVES:**

- To understand modern research processes, ethics, and data-driven decision making.
- To familiarize students with research design, data collection, and analysis methods.
- To develop skills in technical writing, publication, and presentation.
- To create awareness on Intellectual Property Rights and patent systems.
- To introduce contemporary research tools and innovation protection mechanisms.

**COURSE CONTENT:**

| **Unit 1** | **Research Design and Modern Research Approaches** | **9** | **3** | **0** | **12** | **24** | | **1** |
|---|---|---|---|---|---|---|---|---|

Research ecosystem and lifecycle, types of research, problem identification, literature gap analysis, research questions and hypotheses, AI-assisted literature review tools, research design frameworks, qualitative and quantitative research, experimental and survey methods, research ethics and plagiarism awareness.
**Activities:** Literature gap identification, ethics discussion.

| **Unit 2** | **Data Collection, Sources and Preparation** | **9** | **3** | **0** | **12** | **24** | | **3** |
|---|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Primary and secondary data sources, digital and open datasets, measurement scales, questionnaire design, sampling techniques, sample size estimation, data preprocessing, cleaning, transformation, and basic data visualization.<br>**Activities:** Questionnaire design, data visualization exercise. | | | | | | | | |
| **Unit 3** | **Data Analysis, Interpretation and Scientific Communication** | **9** | **3** | **0** | **12** | **24** | | **2** |
| Descriptive and inferential statistics, hypothesis testing, correlation and regression basics, introduction to multivariate analysis, use of analytical tools (Excel/SPSS/Python – overview), interpretation of results, technical report writing, journal and conference paper formats (IEEE/IET), presentation techniques.<br>**Activities:** Data analysis demo, paper formatting. | | | | | | | | |
| **Unit 4** | **Intellectual Property Rights and Innovation Ecosystem** | **9** | **3** | **0** | **12** | **24** | | **7** |
| Concept, meaning, and significance of Intellectual Property Rights (IPR); types of IPR including patents, copyrights, trademarks, industrial designs, and geographical indications; role of IPR in innovation, research, and economic development; overview of national IPR framework with reference to Indian Patent Office and international agreements under World Intellectual Property Organization; importance of IPR in academia, industry, and technology-driven entrepreneurship.<br>**Activities:** IPR case study. | | | | | | | | |
| **Unit 5** | **Patents and Technology Protection** | **9** | **3** | **0** | **12** | **24** | | **2,7** |
| Patent concepts and objectives, patentability criteria, novelty and inventive step, patent specifications, prior art search, types of patent applications, patent filing process, examination and grant, licensing and technology valuation, career opportunities in patent and innovation management.<br>**Activities:** Patent search exercise. | | | | | | | | |
| **COURSE OUTCOMES:** | | | | | | | | |
| **At the end of the course, the students will be able to:**<br>CO1: Apply suitable research methodologies to formulate research problems.<br>CO2: Design data collection instruments and choose appropriate sampling methods.<br>CO3: Analyze and interpret research data using basic analytical tools.<br>CO4: Apply appropriate IP strategies for safeguarding innovations and research outputs.<br>CO5: Apply principles of IPR, patents, and ethical research practices in research and innovation activities. | | | | | | | | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | | | | | | | | |
| **Assessment Methodology:** Internal Assessment Test (70%), Activities (30%) | | | | | | | | |
| **TEXT BOOKS:** | | | | | | | | |

| | |
|---|---|
| 1. | John W. Creswell, J. David Creswell, “Research Design: Qualitative, Quantitative, and Mixed Methods Approaches”, Fifth Edition, Sage Publications, 2023. |
| 2. | Deborah E. Bouchoux, “Intellectual Property: Patents, Trademarks, Copyrights and Trade Secrets”, Fifth Edition, Cengage Learning, 2021. |
| **REFERENCES:** | |
| 1. | Pamela S. Schindler, “Business Research Methods”, Fourteenth Edition, McGraw Hill, 2025. |
| 2. | Deborah E. Bouchoux, “Intellectual Property: Patents, Trademarks, Copyrights and Trade Secrets”, Fifth Edition, Cengage Learning, 2021. |
| 3. | David Hitchcock, “Patent Searching Made Easy”, Second Edition, Routledge, 2020. |
| 4. | Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, Joseph Bizup, William T. FitzGerald, “The Craft of Research”, Fifth Edition, University of Chicago Press, 2024. |
| 5. | V.K. Ahuja, “Intellectual Property Rights: Law and Practice”, Third Edition, LexisNexis, 2022. |
| **E resources/E materials:** | |
| 1. | WIPO IP Portal – Online learning modules on Intellectual Property Rights and patents.( https://www.wipo.int/academy) |
| 2. | Google Scholar – Scholarly literature search and citation tracking platform. (https://scholar.google.com ) |
| 3. | Indian Patent Office (IPO) Website – Patent search, filing procedures, and legal guidelines. (https://ipindia.gov.in) |

**Mapping of Course Outcomes to Programme Outcomes**

| **Course Outcomes** | **PO** | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 3 | 3 | 2 | 3 | 1 | 1 |
| **CO2** | 3 | 3 | 3 | 2 | 2 | 1 |
| **CO3** | 3 | 3 | 2 | 3 | 3 | 1 |
| **CO4** | 2 | 2 | 3 | 2 | 2 | 3 |
| **CO5** | 2 | 2 | 2 | 2 | 1 | 3 |
| **CO** | 3 | 3 | 2 | 2 | 2 | 2 |

| RM26C02 | Research Tool Laboratory | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 0 | 0 | 60 | 0 | 60 | 2 | 4,9,16,17 |

**COURSE OBJECTIVES:**

- To provide hands-on training in modern research and project management tools.
- To develop skills in literature review, reference management, and plagiarism checking.
- To train students in research paper formatting, writing, and publication workflow.
- To introduce data analysis and visualization tools for research applications.
- To enable preparation of professional research reports and technical presentations.

**LIST OF ACTIVITIES:**

1. Research Planning and Project Management
1.1 Research lifecycle, milestones, and project planning
1.2 Gantt chart preparation using MS Project / Notion / OneNote

2. Literature Review and Reference Management
2.1 Advanced literature search using Google Scholar / Scopus
2.2 Reference management using Mendeley / Zotero

3. Research Problem Identification
3.1 Literature gap analysis, AI-assisted literature gap analysis
3.2 Research problem, objectives, and hypothesis formulation

4. Research Paper Formatting
4.1 IEEE / IET journal and conference templates
4.2 Professional writing using Overleaf, Grammarly

5. Publication Workflow
5.1 Journal selection using Elsevier Journal Finder
5.2 Peer review process and reviewer response simulation

6. Data Analysis – Basic Tools
6.1 Data entry, cleaning, and preprocessing
6.2 Descriptive statistics and graphical visualization

7. Data Analysis – Advanced Tools
7.1 Introduction to SPSS / MATLAB for research analysis
7.2 Interpretation of results and inference

8. Plagiarism Detection and Research Ethics
8.1 Plagiarism checking using Turnitin / Urkund
8.2 Ethical paraphrasing and citation practices

9. Referencing and Citation Standards
9.1 IEEE, APA referencing styles
9.2 Automated citation generation and consistency check

10. AI in Research and Automation
10.1 AI tools for research assistance, ChatGPT, Perplexity AI -Automated summarization, idea generation
10.2 Ethical use of AI in research

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**
CO1: Plan and manage research activities using modern research tools.
CO2: Conduct systematic literature review and manage references effectively.
CO3: Analyze and interpret research data using suitable software tools.
CO4: Prepare plagiarism-free research papers and technical reports.
CO5: Present research findings professionally through reports and presentations.

**Weightage:** Continuous Assessment: 60%, End Semester Examinations: 40%

**Assessment Methodology:** Evaluation of Student's work, Observation, Record, Activities etc. (75%), Model Practical Exam (25%)

**REFERENCES:**


| | |
|---|---|
| 1. | Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, Joseph Bizup, William T. FitzGerald , "The Craft of Research", Fifth Edition, University of Chicago Press, 2024. |
| 2. | John W. Creswell, J. David Creswell, "Research Design: Qualitative, Quantitative, and Mixed Methods Approaches", Fifth Edition, SAGE Publications, 2023. |
| 3. | Mark N. K. Saunders, Philip Lewis, Adrian Thornhill , "Research Methods for Business Students" , Ninth Edition, Pearson Education, 2023. |
| 4. | Herman Aguinis, "Research Methodology: Best Practices for Rigorous, Credible, and Impactful Research", SAGE Publications, 2025. |
| 5. | Jiawei Han, Micheline Kamber, Jian Pei, "Data Mining: Concepts and Techniques", Third Edition, 2025. |


**E resources/E materials:**

| | |
|---|---|
| 1. | Reference organization, citation generation, PDF management https://www.mendeley.com |
| 2. | Collaborative LaTeX writing for research papers https://www.overleaf.com. |

| | |
|---|---|
| 3. | Plagiarism detection and originality reports https://www.turnitin.com. |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 2 | 3 | 3 | 3 | 1 |
| **CO2** | 2 | 3 | 2 | 3 | 3 | 1 |
| **CO3** | 3 | 3 | 2 | 3 | 3 | 1 |
| **CO4** | 2 | 2 | 3 | 2 | 2 | 3 |
| **CO5** | 2 | 2 | 2 | 2 | 2 | 2 |
| **CO** | 2 | 2 | 2 | 3 | 3 | 2 |

| **VL26104** | **Analog IC Design Laboratory** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **0** | **0** | **60** | **0** | **60** | **2** | **4,7,9,12,13** |

**COURSE OBJECTIVES:**

- To learn industry standard Analog IC design
- To learn practical design of Analog amplifiers, current mirror etc.
- To learn the art of analog layout in IC design

**LIST OF ACTIVITIES:**

1. Simulation of MOSFET IV characteristics and Extraction of second order parameters.
2. Design and Analysis of CMOS inverter.
3. Design and Analysis of basic single stage amplifiers (common source, common gate and common drain)
4. Design and Analysis of differential amplifier with active load and current source load
5. Design and Analysis of simple current mirror and cascode current mirror.
6. Design and Analysis of two stage op-amp with frequency compensation
7. Realize layout of CMOS inverter and perform post layout simulation.
8. Realize layout of CS amplifier with active load, with NMOS transistor as drive and PMOS transistor as load and perform post layout simulation.

**LAB REQUIREMENTS**

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Use EDA tools for Circuit Design

| | |
|---|---|
| CO2: Design analog Circuit using CMOS given a design specification.<br>CO3: Design and carry out time domain and frequency domain simulations of simple analog building blocks.<br>CO4: Perform Pre-Layout Simulation and Post-Layout Simulation in analog circuits. | |
| **Weightage:** Continuous Assessment: 60%, End Semester Examinations: 40% | |
| **Assessment Methodology:** Evaluation of Student's work, Observation, Record, Activities etc.(75%), Model Practical Exam (25%) | |
| **REFERENCES:** | |
| 1. | Tertulien Ndjountche, "CMOS Analog Integrated Circuits: High-Speed and Power-Efficient Design", Second Edition, CRC Press, 2020. |
| 2. | James M. Fiore, "Operational Amplifiers & Linear Integrated Circuits: Theory and Application", Third Edition, West Publishing, 2021. |
| 3. | Boris Murmann, "Analysis and Design of Elementary MOS Amplifier Stages", Third Edition, National Technology and Science Press, 2022. |
| **E resources/E materials:** | |
| 1. | https://picture.iczhiku.com/resource/eetop/syIGwjYDFqulzbvB.pdf |
| 2. | https://www.nxp.com/docs/en/user-guide/MOSFET-Application-Handbook.pdf |
| 3. | https://web.ece.ucsb.edu/yuegroup/Teaching/ECE2C/Lab/Lab1.pdf |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 1 | 2 | 2 | 2 | 1 |
| **CO2** | 2 | 1 | 2 | 3 | 2 | 1 |
| **CO3** | 2 | 1 | 2 | 3 | 2 | 1 |
| **CO4** | 2 | 1 | 2 | 2 | 2 | 1 |
| **CO** | 2 | 1 | 2 | 3 | 2 | 1 |

| VL26105 | Technical Seminar | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 0 | 0 | 30 | 0 | 30 | 1 | 4,8,9, 16,17 |

**COURSE OBJECTIVES:**

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A technical seminar requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following activities:

**LIST OF ACTIVITIES:**

- Selecting a subject, narrowing the subject into a topic.
- Stating an objective.
- Collecting the relevant bibliography (atleast 15 journal papers).
- Preparing a working outline.
- Studying the papers and understanding the authors contributions and critically analysing each paper.
- Preparing a working outline.
- Linking the papers and preparing a draft of the paper.
- Preparing conclusions based on the reading of all the papers.
- Writing the Final Paper and giving final Presentation.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**
CO1: Identify latest developments in the field of VLSI Design
CO2: Develop technical writing abilities for seminars, conferences and journal publications
CO3: Make use of modern tools to present the technical details

**Weightage:** Review I - 25% & Review II - 25%, Review III: 50%

**Assessment Methodology:** Review (50%), Report (30%), Viva-Voce Examination (20%)

**Method of Evaluation:**

| Activity | Instructions | Submission week | Evaluation |
|---|---|---|---|
| Selection of area of interest and Topic | You are requested to select an area of interest, topic and state an objective | 2nd week | 3% based on clarity of thought, current relevance and clarity in writing |
| Stating an Objective | | | |
| Collecting Information | 1. List 1 Special Interest Groups or professional society | 3rd week | 3% (the selected information must be area specific and of |

| | | | |
|---|---|---|---|
| about your area & topic | 2. List 2 journals<br>3. List 2 conferences, symposia or workshops<br>4. List 1 thesis title<br>5. List 3 web presences (mailing lists, forums, news sites)<br>6. List 3 authors who publish regularly in your area<br>7. Attach a call for papers (CFP) from your area. | | international and national standard) |
| Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter | • You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar<br>• When picking papers to read - try to:<br>• Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them,<br>• Favour papers from well-known journals and conferences,<br>• Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper),<br>• Favour more recent papers,<br>• Pick a recent survey of the field so you can quickly gain an overview,<br>• Find relationships with respect to each other and to your topic area (classification scheme/categorization)<br>• Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered | 4th week | 6% (the list of standard papers and reason for selection) |
| Reading and notes for first 5 papers | Reading Paper Process<br>• For each paper form a Table answering the following questions: What is the main | 5th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your |

| | | | |
|---|---|---|---|
| | topic of the article?<br>• What was/were the main issue(s) the author said they want to discuss?<br>• Why did the author claim it was important?<br>• How does the work build on other's work, in the author's opinion? 5 th week 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)<br>• What simplifying assumptions does the author claim to be making?<br>• What did the author do?<br>• How did the author claim they were going to evaluate their work and compare it to others?<br>• What did the author say were the limitations of their research?<br>• What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey) | | conclusions about each paper) |
| Reading and notes for next 5 papers | Repeat Reading Paper Process | 6th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Reading and notes for final 5 papers | Repeat Reading Paper Process | 7th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Draft outline 1 and Linking papers | Prepare a draft Outline, your survey goals, along with a classification / categorization diagram | 8th week | 8% (this component will be evaluated based on the linking and classification among the papers) |

| | | | |
|---|---|---|---|
| Abstract | Prepare a draft abstract and give a presentation | 9th week | 6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce |
| Introduction Background | Write an introduction and background sections | 10th week | 5% (clarity) |
| Sections of the paper | Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey | 11th week | 10% (this component will be evaluated based on the linking and classification among the papers) |
| Your conclusions | Write your conclusions and future work | 12th week | 5% (conclusions – clarity and your ideas) |
| Final Draft | Complete the final draft of your paper | 13th week | 10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report |
| Seminar | A brief 15 slides on your paper | 14th week & 15th week | 10% (based on presentation and Viva-voce) |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 3 | 2 | 3 | 2 | 2 | 3 |
| **CO2** | 3 | 2 | 3 | 2 | 2 | 3 |
| **CO3** | 3 | 2 | 3 | 2 | 2 | 3 |
| **CO** | 3 | 2 | 3 | 2 | 2 | 3 |

## SEMESTER II

| **VL26201** | **Semiconductor Devices and Modeling** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **7,9,12,13** |
| **COURSE OBJECTIVES:** | | | | | | | | |
| ● To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.<br>● To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications<br>● To acquire the fundamental knowledge of different semiconductor device modelling aspects | | | | | | | | |
| **COURSE CONTENT:** | | | | | | | | |
| **Unit 1** | **MOS Capacitors** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling.<br>**Activities:**1. Problem solving: Analyzing MOS Capacitor Behavior under Different Bias Conditions. | | | | | | | | |
| **Unit 2** | **MOSFET Devices** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |
| MOSFET Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields<br>**Activities:**1. Case Study: Performance Analysis of MOSFET under Short-Channel and High-Field Effects | | | | | | | | |
| **Unit 3** | **CMOS Device Design** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |
| CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V<br>Measurements<br>**Activities:** 1. Quiz: CMOS Scaling and Channel Length Concepts | | | | | | | | |
| **Unit 4** | **Bipolar Devices** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |
| n–p–n Transistors, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor<br>**Activities**:1. Problem solving: Analyze Non-Ideal behaviour of an n–p–n Transistor | | | | | | | | |
| **Unit 5** | **Mathematical Techniques for Device Simulations** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

| |
|---|
| Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.<br>**Activities:1**. Simulation: Simulate a simple 1D semiconductor structure (e.g., pn junction or MOS capacitor) using numerical methods. |
| **COURSE OUTCOMES:** |
| **At the end of the course, the students will be able to:**<br>CO1: Determine the behavior of MOS capacitors under different bias conditions.<br>CO2: Determine MOSFET characteristics using device models.<br>CO3: Implement CMOS scaling and channel design to evaluate threshold voltage and channel length effects<br>CO4: Analyze the characteristics of BJT devices using appropriate circuit models<br>CO5: Examine mathematical models and numerical techniques to interpret semiconductor device behavior |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) |
| **REFERENCES:** |

| | |
|---|---|
| 1. | S. M. Sze and Kwok K. Ng, "Physics of Semiconductor Devices", Wiley, 2021. |
| 2. | S. Wang and X. Wang, "MOS Interface Physics, Process and Characterization". Boca Raton, FL, USA: CRC Press, 2022. |
| 3. | C. Y. Chang and S. M. Sze, "Technology Computer Aided Design: Simulation for VLSI MOSFET", Springer, 2020. |
| 4. | Massimo Rudan, Rossella Brunetti, Susanna Reggiani, "Springer Handbook of Semiconductor Devices". Cham, Switzerland: Springer, 2023. |
| 5. | S. M. Sze and M. K. Lee, "Semiconductor Physics and Devices: An Indian Adaptation", Third Edition. New Delhi, India: Wiley India, 2021. |
| **E resources/E materials:** | |
| 1. | NPTEL -Semiconductor Device Modelling and Simulation |

**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 2 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 1 | 2 | 1 | 1 |

| | | | | | | |
|---|---|---|---|---|---|---|
| **CO3** | 2 | 2 | 1 | 2 | 2 | 2 |
| **CO4** | 2 | 2 | 2 | 1 | 2 | 2 |
| **CO5** | 2 | 2 | 2 | 1 | 2 | 2 |
| **CO** | 2 | 2 | 1 | 2 | 2 | 2 |

| **VL26202** | **VLSI Testing and Verification using UVM** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **4,8,9** |

**COURSE OBJECTIVES:**

- To introduce the VLSI testing.
- To introduce logic and fault simulation and testability measures.
- To study the test generation for combinational and sequential circuit.
- To provide the students complete understanding on UVM testing
- To become proficient at UVM verification.

**COURSE CONTENT:**

| **Unit 1** | **VLSI Testing** | **9** | **0** | **0** | **9** | **18** | | **4,9** |
|---|---|---|---|---|---|---|---|---|

VLSI Testing Process and Test Equipment- Challenges in VLSI Testing - Test Economics and Product Quality- Fault Modelling - Relationship among Fault Models.

**Activities:**

1. Case Study: Analyze testing flow of a chip with block diagram.
2. Quiz: Testing process and fault models.

| **Unit 2** | **Logic and Fault Simulation with Testability Measures** | **9** | **0** | **0** | **9** | **18** | | **4,9** |
|---|---|---|---|---|---|---|---|---|

Simulation for Design Verification and Test Evaluation - Modelling Circuits for Simulation - Algorithms for True Value and Fault Simulation - Scoap Controllability and observability.

**Activities:**

1. Think-Pair-Share: Impact of testability on fault detection efficiency.
2. Flowchart Design**:** Flowcharts for true value simulation and fault simulation algorithms.

| **Unit 3** | **Test Generation for Combinational and Sequential Circuits** | **9** | **0** | **0** | **9** | **18** | | **8,9** |
|---|---|---|---|---|---|---|---|---|

Algorithms and Representations - Redundancy Identification - Combinational ATPG Algorithms - Sequential ATPG Algorithms - Simulation Based ATPG - Genetic Algorithm Based ATPG.

**Activities:**

1. Case study**:** Apply ATPG techniques to generate test vectors for any circuit.

2. Research paper writing**:** Genetic Algorithm-based ATPG techniques for digital circuits.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Universal Verification Methodology (UVM) and TLM** | **9** | **0** | **0** | **9** | **18** | | **8,9** |

Overview- The Typical UVM Test bench Architecture- The UVM Class Library- Transaction-Level Modelling (TLM) - Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation.

**Activities:**

1. Concept map**:** Relationships among UVM components (driver, sequencer, monitor, agent, environment).
2. Case study**:** Design and explain a basic UVM testbench architecture.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **Developing Reusable Verification Components** | **9** | **0** | **0** | **9** | **18** | | **8,9** |

Modelling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage.

**Activities:**

1. Implementation: Design and implement a reusable UVM agent with configurable components.
2. Research paper writing: Reusable verification methodologies and scalable UVM environments.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Utilize fault models and testing principles to analyze VLSI testing flow and quality metrics.
CO2: Compute fault simulation and SCOAP measures for evaluating circuit testability.
CO3: Implement ATPG techniques to generate efficient test vectors and detect faults in digital circuits.
CO4: Develop UVM concept and transaction-level modeling to build a basic UVM testbench.
CO5:Design reusable UVM verification components using TLM, agents, drivers, sequencers, monitors, environments, and test scenarios.

**Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60%

**Assessment Methodology:** Internal Assessment (70%), Activities (30%)

**REFERENCES:**


| | |
|---|---|
| 1. | Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures: Design for Testability" Elsevier, 2021. |

| | |
|---|---|
| 2. | Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2020. |
| 3. | Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press, 2021. |
| 4. | Srivatsa Vasudevan, “Practical UVM: Step by Step Examples with IEEE 1800.2”, Second Edition, R.R. Bowker, 2020. |
| 5 | Accellera Systems Initiative, “Universal Verification Methodology (UVM) 1800.2-2020” Reference Manual, IEEE Standards Association, 2020. |
| **E resources/E materials:** | |
| 1. | NPTEL Digital VLSI Testing - Video lectures and study material. |
| 2. | NPTEL VLSI Design Verification and Test - Video lectures and study material. |
| 3. | https://www.chipverify.com/uvm/uvm-tutorial. |

**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO2** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO3** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO4** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO5** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO** | 2 | 1 | 3 | 3 | 2 | 1 |

| **VL26203** | **Low Power VLSI Design** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **30** | **45** | **120** | **4** | **4,7,9,12** |

**COURSE OBJECTIVES:**

- To identify the sources of power used in an IC.
- To identify the power reduction techniques based on technology independent and technology dependent.
- To describe how power is lost in different MOS logic circuits.
- To choose appropriate techniques to minimize power loss in digital circuits.

- To design memory circuits that use less power.

**COURSE CONTENT:**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 1** | **Power Dissipation in CMOS** | **9** | **0** | **6** | **9** | **24** | | **4,7,9,12** |

Sources of power Dissipation, Physics of Power Dissipation in CMOS FET Devices – Physics of Power Dissipation in MOSFET Devices- Power Dissipation in CMOS – Hierarchy of limits of power – Basic Principle of Low Power Design.

**Activities:**

1. Simulate a CMOS inverter using open-source tools
2. Modify a given CMOS circuit to reduce power using simulation.

**Practical Experiments:**

1. Power Estimation at Circuit, Transistor and Gate Levels in CMOS Logic.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 2** | **Power Optimization** | **9** | **0** | **6** | **9** | **24** | | **4,7,9,12** |

Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, Low Voltage Circuit Design Techniques.

**Activities:**

1. Design basic circuits (inverter, NAND, full adder) using simulation.

**Practical Experiments:**

1. Low Power Optimization Techniques for Combinational CMOS Logic Circuits.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Design of Low Power CMOS Circuits** | **9** | **0** | **6** | **9** | **24** | | **4,7,9,12** |

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques.

**Activities:**

1. Case Study: Power Optimization in a Mobile Processor Unit

**Practical Experiments:**

1. Low Power Optimization Techniques for Sequential CMOS Logic Circuits.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Power Estimation** | **9** | **0** | **6** | **9** | **24** | **4** | **4,7,9,12** |

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis.

**Activities**:

1. Power Analysis simulation using LTspice / ModelSim / Cadence or any open source tool.

**Practical Experiments:**

1. Power Optimization at Register-Transfer Level Using Behavioral Transformations

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **Synthesis and Software Design for Low Power** | **9** | **0** | **6** | **9** | **24** | **4** | **4,7,9,12** |

Synthesis for Low Power – Behavioral Level Transform – Logic level Optimization for Low Power – Software Design for Low Power.

**Activity:**

1. Examine software design strategies for energy-efficient system performance.

**Practical Experiments:**

1. Power Optimization at Algorithmic Level Using Low-Power Computational Techniques.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Apply principles of CMOS operation to evaluate sources of power dissipation in FET devices.
CO2: Implement suitable multiplier architectures to optimize power consumption in VLSI designs.
CO3: Employ low-power techniques in clock and interconnect design to reduce power consumption.
CO4: Apply power estimation techniques at various design levels using simulation and probabilistic methods.
CO5: Develop simple low-power system modules using synthesis and software methods.

**Weightage:** Continuous Assessment: 50%, End Semester Examinations: 50%

**Assessment Methodology:** Theory (30%), Practical (10%), Activities (10%), End Semester Theory Examinations: 50%

**REFERENCES:**


| | |
|---|---|
| 1. | Rohit Dhiman, Rajeevan Chandel, "Nanoscale VLSI: Devices, Circuits and Applications", Springer, 2020. |
| 2. | Shilpi Birla, "Low Power Designs in Nanodevices and Circuits for Emerging Applications", CRC Press, 2023. |
| 3. | Balwinder Raj, "Nanoelectronics: Materials to Chips Design", CRC Press, 2025. |
| 4. | T. S. Arun Samuel, "Tunneling Field Effect Transistors: Design, Modeling and Applications", CRC Press, 2023. |
| 5. | J.B.Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley, 2020. |


**E resources/E materials:**

| | |
|---|---|
| 1. | NPTEL: Low Power VLSI Circuits & Systems https://nptel.ac.in/courses/106105034 |
| 2. | https://vlsiguru.com/blog/low-power-design-methodologies-vlsi |
| 3. | https://resources.system-analysis.cadence.com/blog/msa2021-low-power-design-techniques-for-power-integrity-in-vlsi |

**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 1 | 2 | 3 | 2 | 1 |
| **CO2** | 2 | 1 | 2 | 2 | 2 | 1 |
| **CO3** | 1 | 1 | 2 | 2 | 2 | 1 |
| **CO4** | 1 | 1 | 2 | 3 | 2 | 1 |
| **CO5** | 2 | 1 | 2 | 2 | 3 | 1 |
| **CO** | 2 | 1 | 2 | 2 | 2 | 1 |

| **VL26204** | **Verification Using UVM Laboratory** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **0** | **0** | **60** | **0** | **60** | **2** | **4,9,12** |

**COURSE OBJECTIVES:**

- To design the system with verilog and system Verilog
- To understand testing using Verilog Hardware Description Language
- To practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

**LIST OF ACTIVITIES:**

1. Simulate a simple UVM testbench and DUT
2. Examining the UVM testbench
3. Design and simulate sequence items and sequence
4. Design and simulate a UVM driver and sequencer
5. Design and simulating UVM monitor and agent
6. Design, simulate and examine coverage
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8. Design and simulate a test that runs multiple sequence
9. Design and simulate a configurable UVM test environment

**LAB REQUIREMENTS:** Mentor Graphics QuestaSim / ModelSim/ Cadence/ Synopsys.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Use System Verilog and UVM concepts to simulate a basic testbench and verify a simple DUT.
CO2: Develop UVM components such as sequence items, sequences, driver, and sequencer.
CO3: Construct UVM components including monitor, agent, and environment for functional

| | |
|---|---|
| verification.<br>CO4: Implement coverage collection and scoreboard mechanisms to analyze and verify DUT functionality.<br>CO5: Design a configurable UVM test environment to execute multiple test scenarios and validate system behavior. | |
| **Weightage:** Continuous Assessment: 60%, End Semester Examinations: 40% | |
| **Assessment Methodology:** Evaluation of Student's work, Observation, Record, Activities etc.(75%), Model Practical Exam (25%) | |
| **REFERENCES:** | |
| 1. | Srivatsa Vasudevan, "Practical UVM: Step by Step Examples with IEEE 1800.2", R.R. Bowker, Second Edition, 2020. |
| 2. | Ray Salemi, "The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology", Boston Light Press, 2021. |
| 3. | Erik Seligman, Tom Schubert, Miro Filipovic**, "**Formal Verification: An Essential Toolkit for Modern VLSI Design", Springer**,** 2021**.** |
| **E resources/E materials:** | |
| 1. | https://www.chipverify.com/uvm/uvm-tutorial. |

**Mapping of Course Outcomes with Programme Outcomes**

| **Course Outcomes** | **PO** | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 1 | 3 | 2 | 2 | 1 |
| **CO2** | 2 | 1 | 3 | 2 | 2 | 1 |
| **CO3** | 2 | 1 | 3 | 2 | 2 | 1 |
| **CO4** | 2 | 1 | 3 | 2 | 2 | 1 |
| **CO5** | 2 | 1 | 3 | 2 | 2 | 1 |
| **CO** | 2 | 1 | 3 | 2 | 2 | 1 |

# Open Elective -I

| VL26901 | VLSI Technology | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 0 | 0 | 45 | 90 | 3 | 3, 4, 8, 9 |

**COURSE OBJECTIVES:**

- To understand the fundamentals of silicon crystal growth, wafer preparation, and material properties used in VLSI fabrication.
- To examine epitaxy and thin-film deposition techniques used in semiconductor manufacturing.
- To apply oxidation and diffusion principles for controlling dopant profiles and semiconductor properties.
- To evaluate lithography, etching, and metallization techniques for VLSI fabrication.
- To integrate bipolar, NMOS, and CMOS fabrication processes for VLSI process development.

**COURSE CONTENT:**

| Unit 1 | Crystal Growth and Wafer Preparation | 9 | 0 | 0 | 9 | 18 | | 4, 8, 9 |
|---|---|---|---|---|---|---|---|---|

Electronic grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Processing Considerations.
**Activities:** 1.Compare Czochralski crystal growth and wafer preparation techniques and recommend a suitable process for a specified VLSI application.

| Unit 2 | Epitaxy and Polysilicon Film Deposition | 9 | 0 | 0 | 9 | 18 | | 4, 8, 9 |
|---|---|---|---|---|---|---|---|---|

Vapor -Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Deposition Process, Plasma assisted Deposition.
**Activities:** 1.Conduct a quiz on epitaxy techniques, silicon-on-insulator structures, polysilicon deposition, and plasma-assisted deposition.

| Unit 3 | Oxidation and Diffusion | 9 | 0 | 0 | 9 | 18 | | 4, 8, 9 |
|---|---|---|---|---|---|---|---|---|

Growth Mechanism and Kinematics, Oxidation Techniques and Systems, Oxidation of Polysilicon, Models of Diffusion in Solid, Fick's One-Dimensional Diffusion Equations, Atomistic Diffusion Mechanisms.
**Activities:** 1. Create a concept map linking oxidation mechanisms, oxidation techniques, diffusion models, Fick’s laws, and dopant profiles.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Lithography, Etching and Metallization** | **9** | **0** | **0** | **9** | **18** | | **4, 8, 9** |
| Lithographic process, Optical Lithography, Electron beam Lithography, Dry etching process for VLSI technology, Metallization Problems, Metallization Failure.<br>**Activities**: 1.Compare optical/e-beam lithography, wet/dry etching, and metallization techniques based on process requirements and fabrication challenges. | | | | | | | | |
| **Unit 5** | **VLSI Process Integration** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
| Fundamental Considerations for IC Processing, Bipolar IC Technology NMOS IC Technology, CMOS IC Technology, Modern IC Fabrication.<br>**Activities:** 1. Construct a process flow diagram showing the major fabrication steps involved in CMOS technology, from wafer preparation to final metallization. | | | | | | | | |
| **COURSE OUTCOMES:** | | | | | | | | |
| **At the end of the course, the students will be able to:**<br>**CO1:** Demonstrate the selection of crystal growth and wafer preparation techniques for specified VLSI fabrication requirements.<br>**CO2:** Differentiate epitaxy and thin-film deposition techniques based on their process parameters and fabrication requirements.<br>**CO3:** Determine suitable oxidation and diffusion conditions for achieving required dopant profiles in semiconductor devices.<br>**CO4:** Evaluate lithography, etching, and metallization techniques for addressing VLSI fabrication requirements.<br>**CO5:** Integrate bipolar, NMOS, and CMOS process steps to formulate suitable VLSI fabrication sequences. | | | | | | | | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | | | | | | | | |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) | | | | | | | | |
| **REFERENCES:** | | | | | | | | |
| 1. | Ulrich Hilleringmann, “Silicon Semiconductor Technology: Processing and Integration of Microelectronic Devices”, 1st Edition, Springer, 2023. | | | | | | | |
| 2. | Yaguang Lian, Semiconductor Microchips and Fabrication: A Practical Guide to Theory and Manufacturing, Wiley, 2022. | | | | | | | |
| 3. | Shubham Kumar and Ankaj Gupta, “Integrated Circuit Fabrication”, 1st Edition, CRC Press/Routledge, 2021. | | | | | | | |

| | |
|---|---|
| 4. | V. Suresh Kumar, Ajay Balwantrao Thatere, M. Madhu Babu, A. Arunkumar Gudivada, " VLSI Technology" 1st Edition, BR Publications, 2025. |
| 5 | Brundavani P, Abdul Raheem B, Rachapudi Prabhakar "An introduction to VLSI Design and Testing: Crafting Tommorrow's Technology through VLSI", Garuda Publishers, 2026. |
| **E resources/E materials:** | |
| 1. | Nptel Course : Fundamentals of electronic device fabrication https://nptel.ac.in/ courses/113106062 |
| 2. | Nptel Course : Basic Overview of Semiconductor Device Processing and IC Fabrication, https://nptel.ac.in/courses/108104865 |

**Mapping of Course Outcomes with Program Outcomes**

| Course Outcomes | Programme Outcomes | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO2** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO3** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO4** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO5** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO** | 2 | 2 | 2 | 1 | 1 | 2 |

| **VL26902** | **Embedded System Design** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **3, 4, 8, 9** |

**COURSE OBJECTIVES:**

- To apply embedded system design methodologies for addressing design constraints and performance requirements.
- To analyze processor architectures, memory systems, and peripherals used in embedded systems.
- To analyze bus structures and communication protocols for embedded system interfacing.
- To apply state-machine and concurrent-process models for embedded system development.
- To design real-time embedded systems using appropriate software, RTOS, and hardware resources.

**COURSE CONTENT:**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 1** | **Embedded System Overview** | **9** | **0** | **0** | **9** | **18** | | **4, 8, 9** |
| Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.<br>**Activities:** 1.Analyze a real-world embedded system and optimize its architecture based on performance, power, cost, size, and reliability constraints. | | | | | | | | |
| **Unit 2** | **General and Single Purpose Processor** | **9** | **0** | **0** | **9** | **18** | | **4, 8, 9** |
| Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.<br>**Activities:** 1.Compare processor architectures, microcontrollers, and peripheral interfaces to select suitable components for a given embedded system application. | | | | | | | | |
| **Unit 3** | **Bus Structures** | **9** | **0** | **0** | **9** | **18** | | **8, 9** |
| Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.<br>**Activities:** 1. Analyze and compare I²C, CAN, USB, Bluetooth, and IEEE 802.11 protocols to select the most suitable communication protocol for a given embedded application. | | | | | | | | |
| **Unit 4** | **State Machine and Concurrent Process Models** | **9** | **0** | **0** | **9** | **18** | | **3, 8, 9** |
| Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.<br>**Activities**: 1. Develop a state-machine and concurrent-process model for a real-time embedded application using RTOS concepts. | | | | | | | | |
| **Unit 5** | **System Design** | **9** | **0** | **0** | **9** | **18** | | **3, 8, 9** |
| Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements -Designing the codecs -The overall system design.<br>**Activities:**1. Design an embedded security or audio system by analyzing design requirements, software development, emulation, and system integration. | | | | | | | | |

| COURSE OUTCOMES: | |
|---|---|
| **At the end of the course, the students will be able to:**<br>CO1: Apply embedded system architectures, design constraints, processors, memory, and peripheral components for a given application.<br>CO2: Implement processor, memory, and peripheral interfacing techniques to develop embedded system solutions.<br>CO3**:** Analyze wired and wireless communication protocols and select suitable bus structures for embedded applications.<br>CO4: Demonstrate state-machine, concurrent-process, and RTOS concepts through real-time embedded applications.<br>CO5: Design embedded systems by integrating hardware, software, communication interfaces, and real-time operating system components for real-world applications | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) | |
| **REFERENCES:** | |
| 1. | Lawrence J. Henschen, Julia C. Lee, *"*Embedded System Design Methodologies and Issues*"*, Morgan Kaufmann, 2023. |
| 2. | Raj Kamal, "Embedded Systems: SoC, IoT, AI and Real-time Systems", McGraw Hill Education, 2020. |
| 3. | Santanu Chattopadhyay, "Embedded Systems: Introduction to Arm Cortex-M Microcontrollers", Third Edition, PHI Learning, 2022. |
| 4. | Peter Marwedelis, "Embedded System Design: A Unified Introduction to Cyber-Physical Systems and the Internet of Things", Springer, 2021. |
| 5 | KCS Murti, "Design Principles for Embedded Systems", Springer nature, 2022. |
| **E resources/E materials:** | |
| 1. | Nptel Course : Introduction to Embedded System Design, https://nptel.ac.in/courses / 108102169 |
| 2. | Nptel Course :Embedded Systems Design, https://nptel.ac.in/courses/106105159 |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | Programme Outcomes | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 1 | 1 | 2 | 2 | 3 | 1 |
| **CO2** | 1 | 1 | 2 | 2 | 3 | 1 |
| **CO3** | 1 | 1 | 2 | 2 | 3 | 1 |
| **CO4** | 1 | 1 | 2 | 2 | 3 | 1 |
| **CO5** | 1 | 1 | 2 | 2 | 3 | 1 |
| **CO** | 1 | 1 | 2 | 2 | 3 | 1 |

## PROFESSIONAL ELECTIVE-I

| **VL26001** | **Digital CMOS VLSI Design** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **3, 4, 8, 9** |

**COURSE OBJECTIVES:**

- To learn the CMOS basics in digital circuits.
- To design CMOS-based combinational circuits.
- To design CMOS-based sequential circuits.
- To apply various CMOS logic styles and techniques to optimize digital subsystems.
- To evaluate and estimate circuit performance.

**COURSE CONTENT:**

| **Unit 1** | **MOS Transistors and CMOS Inverter** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
|---|---|---|---|---|---|---|---|---|

MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.
**Activities:** 1. Quiz on Transistors and their characteristics.

| **Unit 2** | **Combinational Logic Circuits** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
|---|---|---|---|---|---|---|---|---|

Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.
**Activities:** 1. Assignment on Design of combinational logic using different CMOS styles.

| **Unit 3** | **Sequential Circuits** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
|---|---|---|---|---|---|---|---|---|

Static latches and registers, dynamic latches and registers, flip-flops, clocking strategies, Schmitt trigger, monostable, astable circuits.
**Activities:** 1. Assignment on Implement various flip-flops and compare timing behavior.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **CMOS Sub System Design** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
| Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.<br>**Activities:** 1. Assignment on Fast multipliers. | | | | | | | | |
| **Unit 5** | **Performance Estimation and Design Techniques** | **9** | **0** | **0** | **9** | **18** | | **3, 4, 8, 9** |
| Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.<br>**Activities:** 1. Seminar on Estimate delay and power for synchronous and self-timed circuit design. | | | | | | | | |
| **COURSE OUTCOMES:** | | | | | | | | |
| **At the end of the course, the students will be able to:**<br>CO1: Demonstrate CMOS basics in digital circuits.<br>CO2: Design CMOS-based combinational circuits.<br>CO3: Design CMOS-based sequential circuits.<br>CO4: Apply various CMOS logic styles and techniques to optimize digital subsystems.<br>CO5: Evaluate and estimate circuit performance. | | | | | | | | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | | | | | | | | |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) | | | | | | | | |
| **REFERENCES:** | | | | | | | | |
| 1. | Weste, N. H. E., & Harris, D., "CMOS VLSI design: A circuits and systems perspective", Fifth edition, Pearson, 2023. | | | | | | | |
| 2. | Karim Abbas," Handbook of Digital CMOS Technology, Circuits, and Systems", Springer Nature, 2020. | | | | | | | |
| 3. | Rohit Dhiman, Rajeevan Chandel," Nanoscale VLSI Devices, Circuits and Applications: Devices, Circuits and Applications", Springer Nature, 2020. | | | | | | | |
| 4. | Manoj Kumar Majumder, Vijay Rao Kumbhare, Aditya Japa, Brajesh Kumar Kaushik, "Introduction to Microelectronics to Nanoelectronics Design and Technology", CRC Press 2023. | | | | | | | |
| 5. | Itamar Levi, Alexander Fish, "Dual Mode Logic A New Paradigm for Digital IC Design", Springer Nature, 2021. | | | | | | | |
| **E resources/E materials:** | | | | | | | | |
| 1. | nptel.ac.in/courses/108107129 | | | | | | | |
| 2. | nptel.ac.in/courses/117106092 | | | | | | | |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO2** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO3** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO4** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO5** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO** | 1 | 2 | 2 | 2 | 1 | 1 |

| **VL26002** | **RF IC Design** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **4,7,9, 11,12** |

**COURSE OBJECTIVES:**

- To extend knowledge of semiconductor devices to analyze MOSFET behavior, noise, and RF transceiver architectures.
- To build on analog circuit fundamentals to design RF front-end circuits and impedance matching networks.
- To apply feedback and amplification concepts in designing RF amplifiers for efficiency, linearity, and stability.
- To translate signal and frequency concepts into the design of RF mixers and oscillators.
- To integrate system-level understanding to model and analyze PLL-based frequency synthesizers.

**COURSE CONTENT:**

| **Unit 1** | **RF Device Physics & Transceiver Architectures** | **9** | **0** | **0** | **9** | **18** | | **4,7,9, 11,12** |
|---|---|---|---|---|---|---|---|---|

Deep-submicron MOSFET models (short-channel, velocity saturation) -RF CMOS vs FinFET vs FD-SOI - Noise in RFICs (thermal, flicker, induced gate noise) -RF performance metrics: NF, IIP2, IIP3, SFDR, EVM - Phase noise (Leeson's model) - Receiver architectures: Zero-IF, Low-IF, Weaver - mmWave transceivers and beamforming - Link budget and specification allocation

**Activities:** 1. Numerical Exercise**:** Calculation of NF and IIP3 for a cascaded RF system.
2. Quiz**:** Noise mechanisms and RF performance metrics.

| **Unit 2** | **Impedance Matching & Low Noise Amplifiers** | **9** | **0** | **0** | **9** | **18** | | **4,7,9, 11,12** |
|---|---|---|---|---|---|---|---|---|

S-parameters, stability (K-factor) - Smith Chart design - Passive RF components (on-chip inductors, varactors) - LNA design: Common source, cascode, common gate, Source degeneration, Noise

matching vs power matching - Bandwidth enhancement techniques

**Activities:**1. Design Exercise: Smith Chart–based impedance matching for an LNA (input/output matching).

2. Think pair share: Trade-off between noise matching and power matching.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Feedback Systems & Power Amplifiers** | **9** | **0** | **0** | **9** | **18** | | **4,7,9, 11,12** |

Feedback theory (gain/phase margin, stability) -RF stability analysis -Power amplifiers: Class A, AB, B, C, D, E, F- Efficiency metrics (PAE) -Linearity improvement: Digital predistortion, Envelope tracking

**Activities:** 1. Case Study: Analysis of Class A vs Class AB vs Class E PA for efficiency and linearity.

2. Simulation Task: Evaluate stability (gain/phase margin) of an RF amplifier with feedback.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Mixers & Oscillators** | **9** | **0** | **0** | **9** | **18** | | **4,7,9, 11,12** |

Mixer fundamentals: Passive vs active, Gilbert cell, Subsampling mixers - Conversion gain, isolation, linearity - Oscillators: LC oscillators, Ring oscillators, Negative resistance concept - Phase noise in oscillators- Frequency dividers.

**Activities**:1. Concept Map Activity: Compare ring vs LC oscillators based on stability, phase noise, power, tuning range, and RF applications.

2. Journal Reference: Comparative study of LC and ring oscillators for RF applications based on phase noise.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **PLL & Frequency Synthesizers** | **9** | **0** | **0** | **9** | **18** | | **4,7,9, 11,12** |

PLL basics and linear model- Phase detectors (PFD, TDC) - Charge pump and loop filter design - Integer-N and Fractional (N PLL) - All-Digital PLL (ADPLL) - Frequency synthesis techniques (DDS) - Noise in PLL systems

**Activities:**1. Case Study: Comparative analysis of Integer-N and Fractional-N PLLs based on resolution, phase noise, complexity, and application suitability.

2. Research Review: Review of recent phase noise reduction techniques in PLL-based frequency synthesizers using IEEE journal references.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Design RF front-end architectures (Zero-IF, Low-IF, mmWave) for wireless communication systems with optimized performance metrics.

CO2: Analyze and optimize MOSFET-based RF circuits considering short-channel effects, noise, and high-frequency limitations.

| |
|---|
| CO3: Design and evaluate RF amplifiers (LNA and PA) achieving trade-offs between gain, noise, linearity, and efficiency.<br>CO4: Develop mixer and oscillator circuits meeting conversion gain, phase noise, and frequency stability requirements.<br>CO5: Design and analyze PLL-based frequency synthesizers for RF communication systems with phase noise and stability constraints. |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) |
| **REFERENCES:** |

| | |
|---|---|
| 1. | D. Leblebici and Y. Leblebici, "Fundamentals of High-Frequency CMOS Analog Integrated Circuits", Second Edition, Springer, Cham, Switzerland, 2021. |
| 2. | Behzad Razavi, "Design of CMOS Radio-Frequency Integrated Circuits", Third Edition,Cambridge University Press, 2021. |
| 3. | R. Sobot, "Wireless Communication Electronics", Second Edition, Springer, Cham, Switzerland, 2021. |
| 4. | John W. M. Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", Third Edition, Artech House, 2022. |
| 5. | Sangeeta Singh, Rajeev Kumar Arya, B. C. Sahana, and Ajay Kumar Vyas (Eds.), "RF Circuits for 5G Applications: Designing with mmWave Circuitry", Wiley-Scrivener, John Wiley &Sons, Hoboken, NJ, USA, 2023. |
| **E resources/E materials:** | |
| 1. | NPTEL – RF Integrated Circuits, IIT Madras. |
| 2. | MIT Open Courseware – RF Circuit Design, Communication Systems, Analog IC Design |
| 3. | Analog Devices – RF Design Tutorials |

**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 1 | 2 | 3 | 2 | 1 |
| **CO2** | 3 | 1 | 2 | 2 | 2 | 1 |
| **CO3** | 2 | 1 | 3 | 3 | 3 | 1 |
| **CO4** | 2 | 1 | 3 | 3 | 2 | 1 |
| **CO5** | 3 | 2 | 3 | 3 | 3 | 1 |
| **CO** | 2 | 1 | 3 | 3 | 2 | 1 |

| VL26003 | Electromagnetic Interference and Compatibility | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 0 | 0 | 45 | 90 | 3 | 3,7,9,11,12 |

**COURSE OBJECTIVES:**

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the principles of PCB design
- To understand the need for standards and to appreciate measurement methods

**COURSE CONTENT:**

| Unit 1 | EMI/EMC Concepts | 9 | 0 | 0 | 9 | 18 | | 3,7,9,12 |
|---|---|---|---|---|---|---|---|---|

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

**Activities:**1. Case study: Radiation Hazards.

2. Quiz: Conducted and Radiated EMI

| Unit 2 | EMI Coupling Principles | 9 | 0 | 0 | 9 | 18 | | 7,9,12 |
|---|---|---|---|---|---|---|---|---|

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling.

**Activities:**1. Case study: Analyze Common mode and differential mode coupling.

2. Think pair share: Cross talk

| Unit 3 | EMI Control Techniques | 9 | 0 | 0 | 9 | 18 | | 3,7,9,12 |
|---|---|---|---|---|---|---|---|---|

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

**Activities:** 1. Case study: Grounding

2. Concept map activity: Cable Routing

| Unit 4 | EMC Design of PCBs | 9 | 0 | 0 | 9 | 18 | | 7,9,12 |
|---|---|---|---|---|---|---|---|---|

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

**Activities**:1. Case study: Analyze the component selection and mounting.

2. Research paper writing: PCB trace impedance

| Unit 5 | EMI Measurements and Standards | 9 | 0 | 0 | 9 | 18 | | 3,7,9,12 |
|---|---|---|---|---|---|---|---|---|

Need for standards - Civilian EMC standards – Military standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.

**Activities:**1. Case study: Design of test environments.

2. Research paper writing: Human exposure limits to EM fields

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Apply knowledge of the various sources of electromagnetic interference to identify and categorize interference in practical engineering scenarios.

CO2: Identify principles of electromagnetic coupling through apertures to solve basic problems involving field interactions and interference effects.

CO3: Analyze different EMI mitigation techniques, including shielding and grounding, to determine their effectiveness in reducing interference.

CO4: Analyze the design of PCB and Signal Integrity unit

CO5: Examine the need for electromagnetic compatibility (EMC) standards and interpret key EMC measurement methods for compliance evaluation.

**Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60%

**Assessment Methodology:** Internal Assessment (70%), Activities (30%)

**REFERENCES:**


| | |
|---|---|
| 1. | Clayton R. Paul, Mark Steffka, Robert Scully, "Introduction to Electromagnetic Compatibility", Wiley India, Third Edition, 2022. |
| 2. | L. Ashok Kumar, Y. Uma Maheswari, "Electromagnetic Interference and Electromagnetic Compatibility: Principles, Design, Simulation, and Applications", CRC Press, 2023 |
| 3. | Yang Zhao, Wei Yan, Jun Sun, Mengxia Zhou, Zhaojuan Meng. "Electromagnetic Compatibility: Principles and Applications", Springer Singapore, 2021. |
| 4. | P. C. Paolo Stefano Crovetti, "Electromagnetic Interference and Compatibility", MDPI Books, 2021. |
| 5. | Reto B. Keller," Design for Electromagnetic Compatibility", Springer, 2022. |


**E resources/E materials:**

| | |
|---|---|
| 1. | https://onlinecourses.nptel.ac.in/noc25_ee32/preview |
| 2. | https://blp.ieee.org/product/introduction-to-electromagnetic-compatibility/ |
| 3. | https://blp.ieee.org/product/advanced-aspects-of-electromagnetic-compatibility/ |

**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 3 | 1 | 2 | 2 | 1 | 1 |
| **CO2** | 2 | 1 | 2 | 3 | 1 | 1 |
| **CO3** | 2 | 1 | 2 | 2 | 3 | 1 |
| **CO4** | 2 | 3 | 1 | 2 | 1 | 2 |
| **CO5** | 2 | 1 | 1 | 3 | 1 | 2 |
| **CO** | 2 | 1 | 2 | 2 | 1 | 1 |

| **VL26004** | **Physical Design of VLSI** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **3,9,12** |

**COURSE OBJECTIVES:**

- Understand the Basics of physical design flow such as component placement, floor plan, routing area partitioning.
- Study the concepts of algorithms used for optimization and how to apply this algorithm in placement and routing.
- Discuss the Detailed and specialized routing and relevant algorithm.
- Understand the concepts of Compaction.
- Acquire knowledge of VLSI Design Automation.

**COURSE CONTENT:**

| **Unit 1** | **VLSI Physical Design Flow** | **9** | **0** | **0** | **9** | **18** | | **9,12** |
|---|---|---|---|---|---|---|---|---|

Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms Deep sub-micron issues; interconnects modelling and synthesis.

**Activities:**1. Case study: Design and Optimization of a VLSI Chip Layout

2. Quiz: Fundamentals of VLSI Physical Design

| **Unit 2** | **Placement and Routing** | **9** | **0** | **0** | **9** | **18** | | **3,9** |
|---|---|---|---|---|---|---|---|---|

Global Placement and Routing: Introduction and objectives of placement, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, Modern placement algorithms Routing terminology and goals. Dijsktra's algorithm. Global routing in a connectivity graph, Modern global routing, over the cell routing algorithms

**Activities:**1. Case study: Optimization of Placement and Routing in a VLSI Chip

2. Think pair share: Understanding Placement & Routing Trade-offs

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Detailed and Specialized Routing** | **9** | **0** | **0** | **9** | **18** | | **9,12** |

Building the Horizontal and Vertical Constraint Graphs, Left edge algorithm, dog-legging, Switchbox routing, Introduction to area routing, Non - Manhattan routing, Routing in clock networks, clock-tree synthesis

**Activities:** 1. Case study: Channel Routing & Clock Network Optimization in VLSI

2. Quiz: Advanced Routing Techniques in VLSI

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Compaction** | **9** | **0** | **0** | **9** | **18** | | **3,9** |

Basic definitions: One-dimensional mask layout compaction. Constraint graph. Circuit extraction and design rule checking. One-dimensional constraint graph compaction algorithm. Two-dimensional compaction, Recent trends in Compaction.

**Activities:**1. Case study: Optimization of VLSI Layout using Compaction Techniques

2. Research paper writing: Advanced Techniques in VLSI Layout Compaction

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **VLSI Design Automation** | **9** | **0** | **0** | **9** | **18** | | **9** |

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

**Activities:** 1. Case study: End-to-End VLSI Design Flow Using Automation Tools

2. Research paper writing: Emerging Trends in VLSI Design Automation

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Examine the VLSI physical design process including partitioning, placement, routing, and design rule verification.

CO2: Apply placement and global routing algorithms such as min-cut, analytic placement, simulated annealing, and shortest path algorithms.

CO3: Analyze detailed routing techniques including constraint graphs, left-edge algorithm, switchbox routing, and clock tree synthesis.

CO4: Evaluate compaction techniques, circuit extraction methods, and design rule checking fo

optimized VLSI layouts.

CO5: Design and assess VLSI design automation strategies including FPGA design flow, EDA tools, and deep sub-micron considerations.

**Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60%

**Assessment Methodology:** Internal Assessment (70%), Activities (30%)

**REFERENCES:**

| | |
|---|---|
| 1. | Andrew B. Kahng, Jens Lienig, Igor L Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Second Edition, Springer, 2022. |
| 2. | Veena S. Chakravarthi & Shivananda R. Koteshwar, "SoC Physical Design: A Comprehensive Guide", Springer, 2022. |
| 3. | Juergen Teich, "Electronic Design Automation", Springer, 2021. |
| 4. | N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", (Classic Reference), 2020. |
| 5. | Veena S. Chakravarthi, "A Practical Approach to VLSI System-on-Chip Design", Second Edition, Springer, 2022. |
| **E resources/E materials:** | |
| 1. | https://nptel.ac.in/courses/117102062 |
| 2. | https://youtu.be/xeEQdo5MOGo |
| 3. | https://youtu.be/fBU5kwCvnpw |
| 4. | https://youtu.be/6iF3M6h8b7c |
| 5. | https://youtu.be/8b9r8Rk6F2M |

**Mapping of Course Outcomes to Programme Outcomes**

| **Course Outcomes** | **PO** | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 2 | - | - | 1 | 1 |
| **CO2** | 2 | 2 | 2 | 1 | 2 | 1 |
| **CO3** | 2 | 2 | 2 | 2 | 2 | 1 |
| **CO4** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO5** | 2 | 2 | 2 | 1 | 1 | 2 |
| **CO** | 2 | 2 | 2 | 1 | 1 | 1 |

| **VL26005** | **Hardware Software Co-Design for FPGA** | **L** | **T** | **P** | **TW/SL** | **Total** | **C** | **SDG** |
|---|---|---|---|---|---|---|---|---|
| | | **45** | **0** | **0** | **45** | **90** | **3** | **7,9,12,13** |
| **COURSE OBJECTIVES:** | | | | | | | | |
| • To acquire the knowledge about system specification and modelling | | | | | | | | |

- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

**COURSE CONTENT:**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 1** | **System Specification and Modelling** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures.

**Activities:**1. Case Study: Hardware vs Software Partitioning for a Real-Time System

2. Quiz : Embedded systems and Hardware/Software Co-Design

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 2** | **Hardware/Software Partitioning** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

**Activities:**1. Case Study: Optimized HW/SW Partition Using Heuristics

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 3** | **Hardware/Software Co-Synthesis** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

**Activities:** 1. Case Study: Modeling a System Using State-Transition Graph for Co-Synthesis.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 4** | **Prototyping and Emulation** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems.

**Activities**:1. Designing a Target Architecture for a Control-Dominated System

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Unit 5** | **Design Specification and Verification** | **9** | **0** | **0** | **9** | **18** | | **7,9,12,13** |

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Multi-Language Co-Simulation.

**Activities:**1. Mini-Project: System-Level Modeling and Co-Simulation.

**COURSE OUTCOMES:**

**At the end of the course, the students will be able to:**

CO1: Construct embedded system architectures using hardware/software co-design principles.

CO2: Solve hardware/software partitioning problems by applying cost estimation and genetic algorithm-based optimization.

CO3: Implement the principles of hardware-software co-synthesis to partition system functions and optimize performance.

CO4: Analyze functional hardware-software prototypes using modern EDA tools and FPGA-based development platforms.

CO5: Examine concurrency, coordination, interfacing, and system-level modeling using specification languages and co-simulation techniques.

**Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60%

**Assessment Methodology:** Internal Assessment (70%), Activities (30%)

**REFERENCES:**


| | |
|---|---|
| 1. | Bashir I. Morshed, "Embedded Systems – A Hardware-Software Co-Design Approach", Springer, 2021. |
| 2. | Peter Marwedel, "Embedded System Design: Foundations of Cyber-Physical Systems and IoT", Springer, 2021. |
| 3. | K.C.S. Murti, "Design Principles for Embedded Systems", Springer, 2021. |
| 4. | Edward H. Currie, "Mixed-Signal Embedded Systems Design", Springer, 2021. |
| 5. | K.C. Wang, "Embedded and Real-Time Operating Systems", Springer, 2023. |


**Mapping of Course Outcomes with Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 2 | 2 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 1 | 2 | 1 | 1 |
| **CO3** | 2 | 2 | 1 | 2 | 2 | 2 |
| **CO4** | 2 | 2 | 2 | 1 | 2 | 2 |
| **CO5** | 2 | 2 | 2 | 1 | 2 | 2 |
| **CO** | 2 | 2 | 2 | 2 | 2 | 2 |

| VL26006 | CAD for VLSI Design | L | T | P | TW/SL | Total | C | SDG |
|---|---|---|---|---|---|---|---|---|
| | | 45 | 0 | 0 | 45 | 90 | 3 | 3,4,8,9 |

**COURSE OBJECTIVES:**

- To evaluate VLSI design methodologies and VLSI design automation tools.
- To apply data structures and algorithms of VLSI design.
- To analyze algorithms in partitioning and placement.
- To develop algorithms in floor planning and routing.
- To design and simulate algorithms for modelling, simulation and synthesis.

**COURSE CONTENT:**

| Unit 1 | Design Methodologies | 9 | 0 | 0 | 9 | 18 | | 3,4,8,9 |
|---|---|---|---|---|---|---|---|---|

VLSI Design Methodologies - VLSI Design Cycle - New Trends in VLSI Design Cycle - Physical Design Cycle - New Trends in Physical Design Cycle - Design Styles - Review of VLSI Design Automation Tools.
**Activities:** 1. Quiz on IC fabrication process and Design Methodologies.

| Unit 2 | Data Structures and Basic Algorithms | 9 | 0 | 0 | 9 | 18 | | 3,4,8,9 |
|---|---|---|---|---|---|---|---|---|

Data Structures and Algorithms - Algorithmic Graph Theory and Computational Complexity- General Purpose Methods for Combinatorial Optimization.
**Activities:** 1. Assignment on Combinatorial Optimization.

| Unit 3 | Algorithms for Partitioning and Placement | 9 | 0 | 0 | 9 | 18 | | 3,4,8,9 |
|---|---|---|---|---|---|---|---|---|

Layout Compaction - Problem Formulation - Algorithms for Constraint Graph Compaction - Partitioning - Placement - Placement Algorithms.
**Activities:** 1. Assignment on Algorithms for Constraint Graph Compaction.

| Unit 4 | Algorithms for Floor Planning and Routing | 9 | 0 | 0 | 9 | 18 | | 4,9,12 |
|---|---|---|---|---|---|---|---|---|

Floor planning - Problem Formulation - Floor planning Algorithms - Routing - Area Routing - Global Routing- Detailed Routing
**Activities:** 1. Assignment on Detailed Routing

| Unit 5 | Modelling, Simulation and Synthesis | 9 | 0 | 0 | 9 | 18 | | 3,4,8,9 |
|---|---|---|---|---|---|---|---|---|

Simulation - Gate Level Modelling and Simulation - Logic Synthesis and Verification - Binary Decision Diagrams - High Level Synthesis
**Activities:** 1. Seminar on Binary decision diagrams.

| COURSE OUTCOMES: | |
|---|---|
| **At the end of the course, the students will be able to:**<br>CO1: Demonstrate VLSI design methodologies and VLSI design automation tools.<br>CO2: Implement data structures and algorithms of VLSI design.<br>CO3: Execute algorithms in partitioning and placement.<br>CO4: Apply algorithms in floor planning and routing.<br>CO5: Evaluate algorithms for modelling, simulation and synthesis. | |
| **Weightage:** Continuous Assessment: 40%, End Semester Examinations: 60% | |
| **Assessment Methodology:** Internal Assessment (70%), Activities (30%) | |
| **REFERENCES:** | |
| 1. | Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu., "VLSI Physical Design: From Graph Partitioning to Timing Closure", Second Edition, Springer Nature, 2022. |
| 2. | Veena S. Chakravarthi, Shivananda R. Koteshwar," SoC Physical Design - A Comprehensive Guide", Springer Nature, 2022. |
| 3. | Weste, N. H. E.& Harris, D., "CMOS VLSI design: A circuits and systems perspective", Fifth Edition, Pearson, 2023. |
| 4. | Thomas Dillinger, "VLSI Design Methodology Development", Pearson India,2020. |
| 5. | Farimah Farahmandi, M. Sazadur Rahman, Sree Ranjani Rajendran, Mark Tehranipoor, "CAD for Hardware Security", Springer Nature, 2023. |
| **E resources/E materials:** | |
| 1. | http://digimat.in/nptel/courses/video/108107380/L01.html |
| 2. | http://digimat.in/nptel/courses/video/106105161/L01.html |

**Mapping of Course Outcomes to Programme Outcomes**

| Course Outcomes | PO | | | | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** |
| **CO1** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO2** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO3** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO4** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO5** | 1 | 2 | 2 | 2 | 1 | 1 |
| **CO** | 1 | 2 | 2 | 2 | 1 | 1 |